

### REMARKS

In response to the Office Action dated 3 June 2005, the applicants request reconsideration of the above-identified application in view of the following remarks. Claims 1-30 are pending in the application. Claims 1, 6, 7, 14-16, 28, and 30 are rejected. Claims 9-13 and 20-27 are allowed and claims 2-5, 8, 17-19, and 29 are objected to. Claims 1, 4, and 28 will be amended upon entry of the present amendment. No new matter has been added.

#### Allowable Subject Matter

The Office Action indicated that claims 9-13 and 20-27 are allowed. The Office Action also indicated that claims 2-5, 8, 17-19, and 29 would be allowable if rewritten in independent form. The applicant reserves the right to rewrite claims 2-5, 8, 17-19, and 29 in independent form, but believes that all of the claims are allowable in view of the remarks made herein.

#### Rejection of Claims Under §102

Claim 28 was rejected under 35 USC § 102(e) as being anticipated by Houg (U.S. 6,324,596). The applicants respectfully traverse.

Houg issued on November 27, 2001, which is after the filing date of the present application. The applicants do not admit that Houg is prior art, and reserve the right to swear behind Houg at a later date.

Amended claim 28 recites a “method of synchronizing an agent to a simultaneous bidirectional bus.” Houg relates to “providing device status during bus retry operations.”<sup>1</sup> Houg describes a PCI bus system that requires a turnaround cycle 110 to ensure that an AD bus is not driven by two devices at the same time.<sup>2</sup> Houg does not show a simultaneous bidirectional bus as is recited in amended claim 28.

The applicants respectfully submit that Houg does not show all of the features recited in amended claim 28, and that claim 28 is in condition for allowance.

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<sup>1</sup> Houg, Title.

<sup>2</sup> Houg, Column 2, lines 17-20.

Claims 14-16 were rejected under 35 USC § 102(e) as being anticipated by Livolsi (U.S. 6,020,767). The applicants respectfully traverse.

Livolsi issued on February 1, 2000, which less than one year before the filing date of the present application. The applicants do not admit that Livolsi is prior art, and reserve the right to swear behind Livolsi at a later date.

Claim 14 recites a “simultaneous bidirectional port circuit comprising: a data driver having an output impedance control circuit to modify an output impedance of the data driver; and a synchronization circuit to alert a second simultaneous bidirectional port circuit that the output impedance has been modified.”

Livolsi relates to a “settable interface receiver cell.”<sup>3</sup> Livolsi shows a receiver circuit with a settable hysteresis.<sup>4</sup> Livolsi does not show “an output impedance control circuit to modify an output impedance” of a data driver as is recited in claim 14. The inverter 318 of Livolsi is a buffer.<sup>5</sup> Livolsi does not show a separate synchronization circuit as is recited in claim 14. Livolsi just shows a receiver circuit in Figure 1. PCNN is an input signal/pin 101.<sup>6</sup> Livolsi does not show a “simultaneous bidirectional port circuit” as is recited in claim 14.

The applicants respectfully submit that Livolsi does not show all of the features recited in claim 14, and that claim 14 is in condition for allowance. Claims 15-16 are dependent on claim 14, and recite further features with respect to claim 14. For reasons analogous to those stated above, and the features in the claims, the applicants respectfully submit that Livolsi does not show all of the features recited in claims 15-16, and that claims 15-16 are in condition for allowance.

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<sup>3</sup> Livolsi, Title.

<sup>4</sup> Livolsi, column 2, lines 39-65.

<sup>5</sup> Livolsi, column 3, line 16.

<sup>6</sup> Livolsi, column 2, lines 39-54.

Rejection of Claims Under §103

Claims 1, 7, and 30 were rejected under 35 USC § 103(a) as being unpatentable over Garde (U.S. 6,002,882) in view of Livolsi. The applicants respectfully traverse.

Garde issued on December 14, 1999, which less than one year before the filing date of the present application. The applicants do not admit that Garde is prior art, and reserve the right to swear behind Garde at a later date.

Claim 30 is dependent on independent claim 28, and recites further features with respect to claim 28. Claim 28 was not rejected based on Garde or Livolsi. The applicants respectfully submit that claim 30 is in condition for allowance.

Amended claim 1 recites an integrated circuit comprising, among other elements, “a driver in a simultaneous bidirectional port” ..... “such that the driver launches an initial voltage value on” a conductor, and “a receiver in the simultaneous bidirectional port.” Claim 7 is dependent on claim 1, and recites further features with respect to claim 1.

Garde relates to a bidirectional communication port that is not simultaneous.<sup>7</sup> Garde shows high-level block diagrams of a DSP, but does not show a driver or a receiver. Garde does not show a driver that launches an initial voltage value on a conductor as is recited in amended claim 1. Livolsi does not supply all of the elements missing in Garde. Therefore, even as combined, Garde and Livolsi do not show all of the features recited in amended claim 1.

The MPEP requires a suggestion and a reasonable expectation of success for a rejection under 35 USC § 103:

“To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations.”<sup>8</sup>

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<sup>7</sup> Garde, lines bridging columns 6-7; column 7, lines 33-67; column 8, lines 5-6.

<sup>8</sup> MPEP 2143.

The suggestion or motivation to combine references and the reasonable expectation of success must both be found in the prior art.<sup>9</sup>

The Office Action states:

“it would have been obvious ... to have combined the teachings of Livolsi within the system of Garde because it would provide a high speed communication between the devices.”<sup>10</sup>

The Office Action has not identified prior art as being the source of the above-quoted rationale for combining Garde and Livolsi as is required by MPEP 2143. The Office Action has also not identified a reasonable expectation of success in the prior art as is required by MPEP 2143.

Furthermore, Livolsi is a transistor-level disclosure of a circuit, while Garde shows high-level block diagrams of a DSP. The Office Action has not specified where the circuit from Livolsi is to be placed in the blocks of Garde. The Office Action has not shown that such a change at the transistor level in the blocks of Garde would have a reasonable expectation of success.

The applicants respectfully submit that a *prima facie* case of obviousness of claims 1 and 7 has not been established in the Office Action, and that claims 1 and 7 are in condition for allowance.

Claim 6 was rejected under 35 USC § 103(a) as being unpatentable over Garde in view of Livolsi and Houg. The applicants respectfully traverse.

Claim 6 is dependent on claim 1, and recites further features with respect to claim 1. For reasons analogous to those stated above, and the features in the claim, the applicants respectfully submit that claim 6 is not shown or suggested by Garde in view of Livolsi and Houg, and that claim 6 is in condition for allowance.

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<sup>9</sup> MPEP 2143.

<sup>10</sup> Office Action, page 4.

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Title: SIMULTANEOUS BIDIRECTIONAL PORT WITH SYNCHRONIZATION CIRCUIT TO SYNCHRONIZE THE PORT WITH ANOTHER PORT

Assignee: Intel Corporation

**CONCLUSION**

The applicants respectfully submit that all of the pending claims are in condition for allowance, and such action is earnestly solicited. The Examiner is invited to telephone the below-signed attorney at 612-373-6973 to discuss any questions which may remain with respect to the present application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,


MATTHEW B. HAYCOCK ET AL.

By their Representatives,

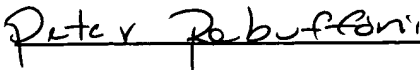
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Date 3 October 2005


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**CERTIFICATE UNDER 37 CFR 1.8:** The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: MS Amendment, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on this 3 day of October, 2005.



Name

  
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